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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,687	12/14/2005	Francesco Pessolano	NL 030671	1945

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EXAMINER	
HUYNH, PHUONG	

ART UNIT	PAPER NUMBER
2857	

NOTIFICATION DATE	DELIVERY MODE
09/08/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	10/560,687	PESSOLANO ET AL.	
	Examiner	Art Unit	
	PHUONG HUYNH	2857	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 07 August 2008 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: _____.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/Eliseo Ramos-Feliciano/
Supervisory Patent Examiner, Art Unit 2857

Continuation of 11. does NOT place the application in condition for allowance because: Regarding claim 1 (Previously was AMENDED), Applicant argues that Buer's COMPARE CIRCUIT 28 does not compare receipt of the output of the duplicate logic path to the receipt of the clock signal in order to produce the timing closure signal as in the claimed invention [see Applicant's Remarks: Page 9, lines 4-7].

Accordingly, as disclosed in Buer, col. 4, lines 10-30, for example, that "he output from the critical path generation circuit 12 and the output of the known path generation circuit 14 are then sent to a comparator circuit 28. The two output signals will be compared by the comparator circuit 28. The known generation path will operate at a much faster rate than the critical path generation circuit 12 since there is very little delay caused by the logic buffer 22. If the two output signals are the same, then the critical path generation circuit 12 is functioning properly. However, if the two signals are different, then the critical path generation circuit 12 is beginning to fail. The comparison is then decoupled by the comparator circuit 28 from the registers 18 and 26 to ensure that there are no meta-stable events in the results. In accordance with one embodiment of the present invention, the decoupling is accomplished through the use of a flip flop. The result of the comparison is then recorded by a counting mechanism within the comparator circuit 28. After a predetermined number of mismatches (i.e., one or more depending on the desire of the user), the comparator circuit 28 will generate a frequency error signal. The counter mechanism of the comparator circuit is used to ensure that the circuit 10 is not continuously causing errors in the system.

Therefore, Buer discloses the claimed "monitoring circuit arranged to receive an output signal from the duplicate logic path, to compare receipt of the output signal relative to receipt of the clock signal, and to provide an output signal indicative of the status of the timing closure in the logic path being monitored".

***Regarding claim 11, Applicant argues that "the cited portions of Buer teach that buffer 22 are not part of critical logic path 20" [see Applicant's Remarks: Page 9, lines 9-18].

Accordingly, Buer discloses in col. 4, lines 9-17, that "The use of an inverting buffer 22A or a non-inverting buffer 22B is based on whether the critical path logic circuit 20 is inverting or non-inverting....". Therefore, Buer meets the claimed "buffer" as recited in claim 11.

****Regarding claims 14 and 16 , Applicant argues that Buer does not disclose "the timing closure violation signal is supplied to a second timing closure monitoring closure monitoring circuits (claim 14)", and "one or more further timing closure monitoring circuits (claim 16" [see Applicant's Remarks: Page 9, lines 20-32].

Buer discloses in col. 4, lines 3-58, that "he frequency error signal generated by the comparator circuit 28 is then sent to a protection circuit 30. The protection circuit 30 has an input coupled to an output of the comparator circuit 28 and an output coupled to an integrated circuit (IC) chip (not shown) for sending a signal to disable the IC chip when the critical path logic circuit 20 begins to fail. In accordance with one embodiment of the present invention, the protection circuit 30 is comprised of a first flip-flop 32 having a first input D coupled to the output of the comparator circuit 28 and a second input coupled to the clock signal CLK for receiving the frequency error signal outputted by the comparator circuit 28. A second flip flop 34 is further provided and has a first input D coupled to an output Q of the first flip flop 32 and a second input coupled to the clock signal CLK. The second flip flop 34 is used for decoupling the frequency error signal to ensure that there are no meta-stable events. A third flip flop 36 is further provided and has an enable input E coupled to an output Q of the second flip flop 34. The third flip flop 36 is used for sending an internal reset signal to disable an IC chip and for continuing to disable the IC chip until a reset signal RST.sub.-- L is sent to the third flip flop 36 to reset and clear the third flip flop 36. Thus if an IC chip is running at a higher frequency than it is suppose to (i.e., failure of the critical path logic circuit 20), the protection circuit 30 will disable the IC chip until the flip flop 36 is reset. Thus at high frequencies, the IC chip cannot run and generate unknown results".

Therefore, Buer discloses the claimed "the timing closure violation signal [freq error] is supplied to a second timing closure monitoring circuit [30] on the integrated circuit, the first and second timing closure monitoring circuits generating a serial interrupt signal".

******Regarding claims 3-6, 8-9, 21-23, 25, and 26 (103 rejections), Applicant argues that "The Examiner asserts that the skilled artisian would be motivated to modify Buer, in some manner which the Examiner does not disclose, in order to "provide an unchanged select signal pulse width. As cited portions of Buer do not mention any selection signal having pusle width" [see Applicant's Remarks: page 10].

Accordingly, This is immaterial. As recited in the Final Office Action, that It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the invention of Buer to include the method, as taught by Chuang, to provide an unchanged select signal pulse width [see Chuang: Paragraphs [0040] and [0046]]". It is Chang who teaches "an unchanged select signal pulse width". Further, Chang's invention is in field of endeavor as required in 103 rejection.